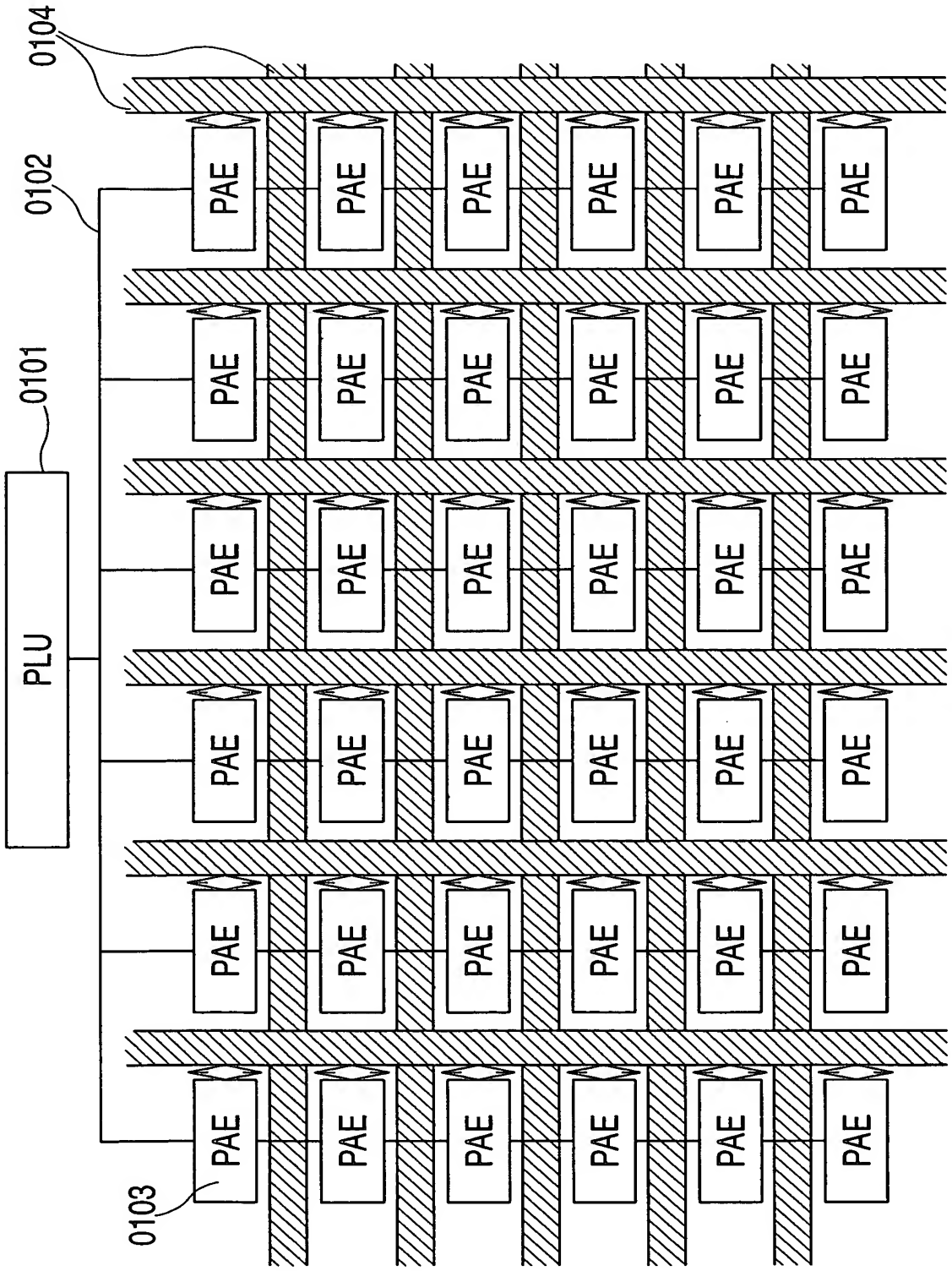

FIG. 1

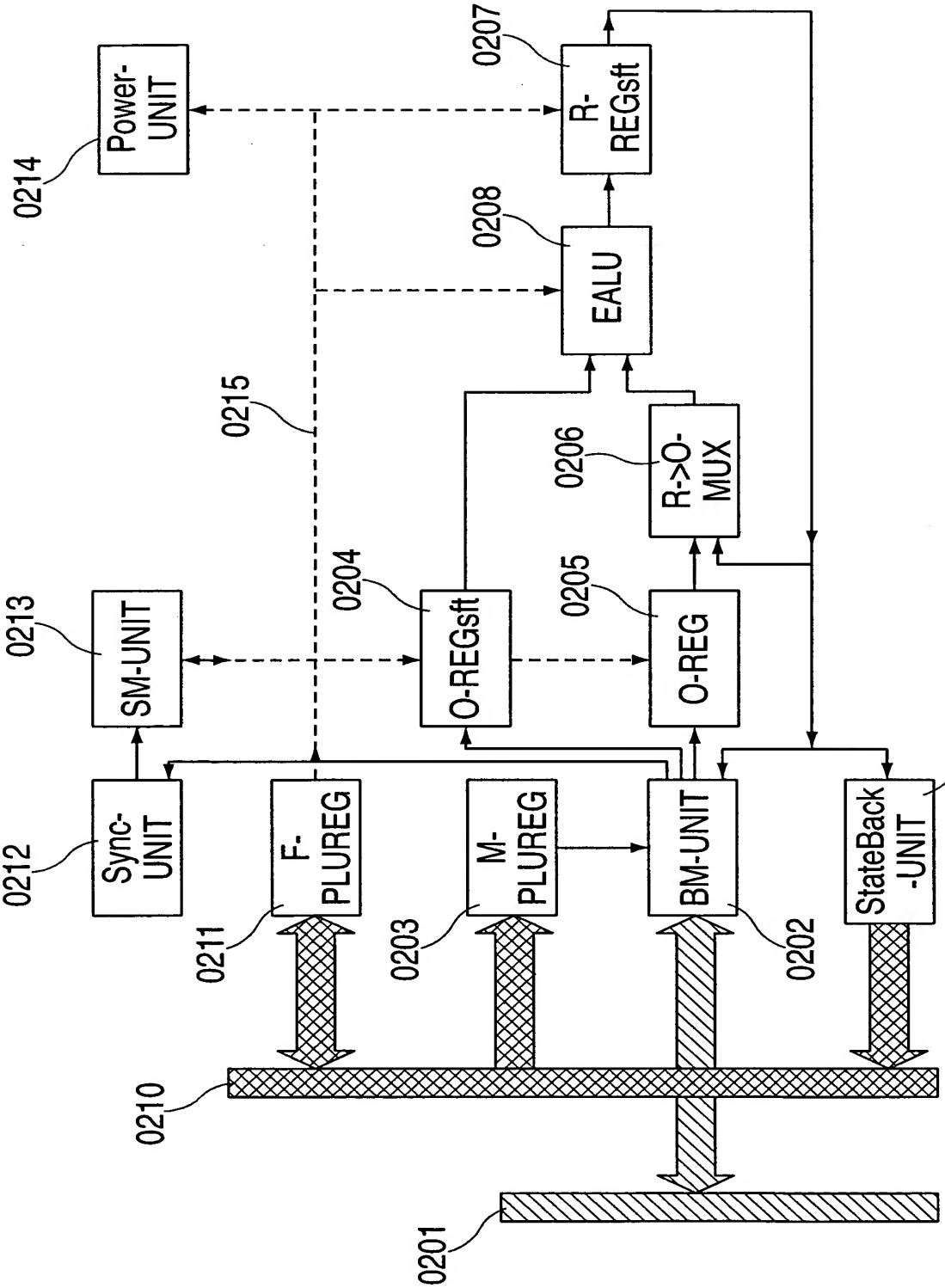
Power-UNIT
0214
0207
R-REGsft
0208
EALU
0215
0206
R->O-MUX
0213
SM-UNIT
0204
O-REGsft
0205
O-REG
0212
Sync-UNIT
0211
F-PLUREG
0203
M-PLUREG
BM-UNIT
0202
StateBack-UNIT
0209
0210
0201

FIG. 2

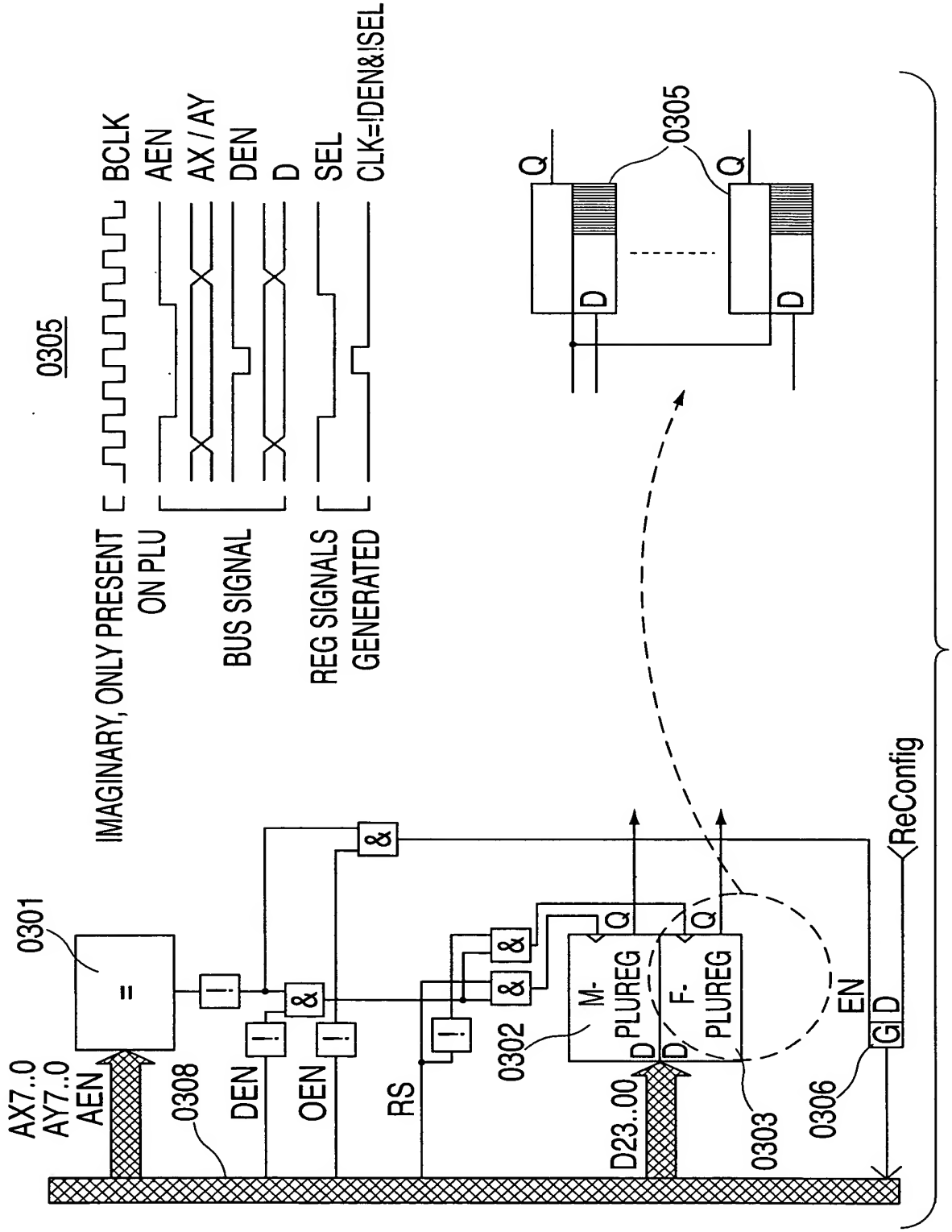
0305
BCLK
AEN
AX / AY
DEN
D
SEL
CLK=!DEN&!SEL
IMAGINARY, ONLY PRESENT ON PLU
BUS SIGNAL
REG SIGNALS GENERATED
Q
D
0305
0301
=
AX7..0
AY7..0
AEN
0308
DEN
OEN
RS
0302
M-PLUREG
F-PLUREG
D23..00
0303
0306
EN
G D
ReConfig

FIG. 3

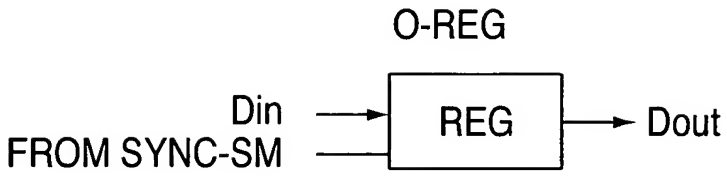

FIG. 4a

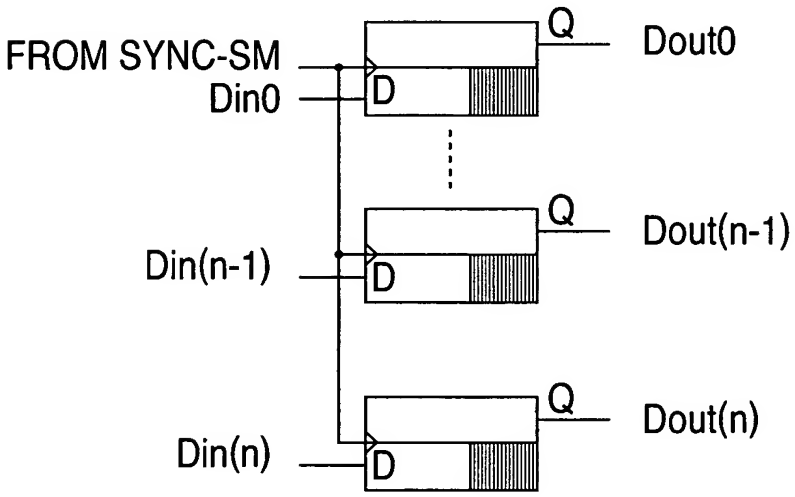

FIG. 4b

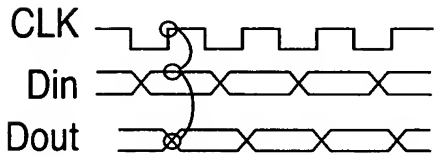

FIG. 4c

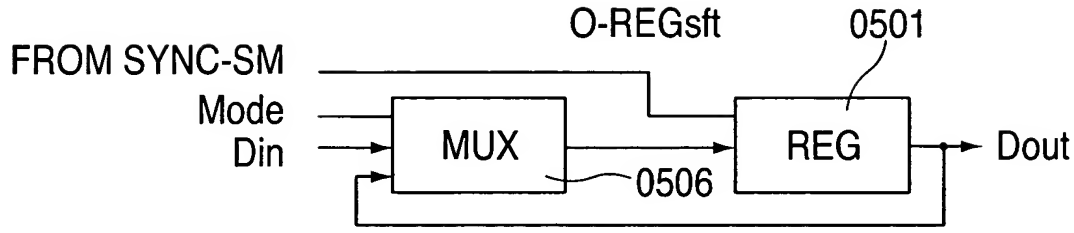

FIG. 5a

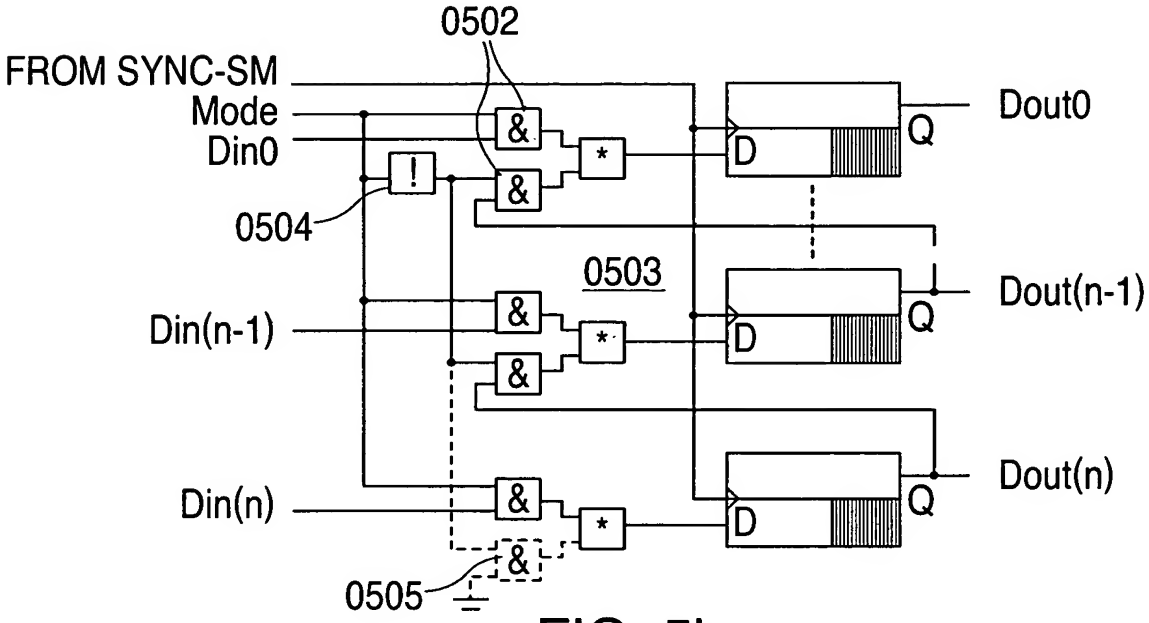

FIG. 5b

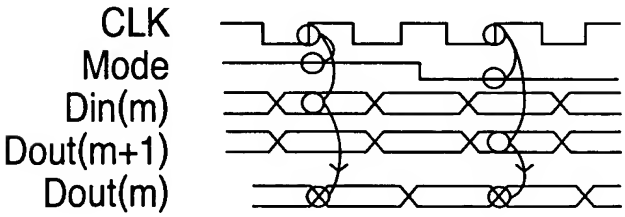

FIG. 5c

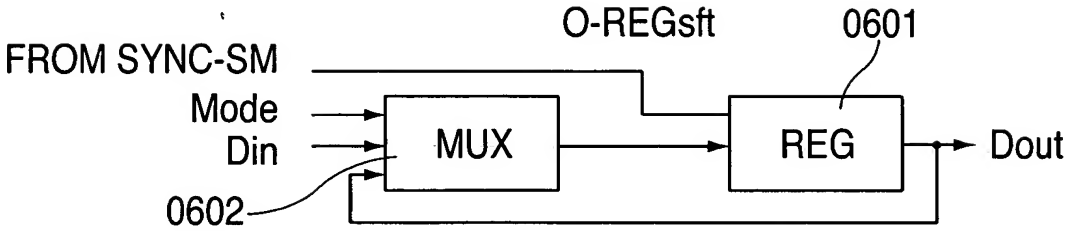
FROM SYNC-SM
Mode
Din
0602
MUX
O-REGsft
0601
REG
Dout

FIG. 6a

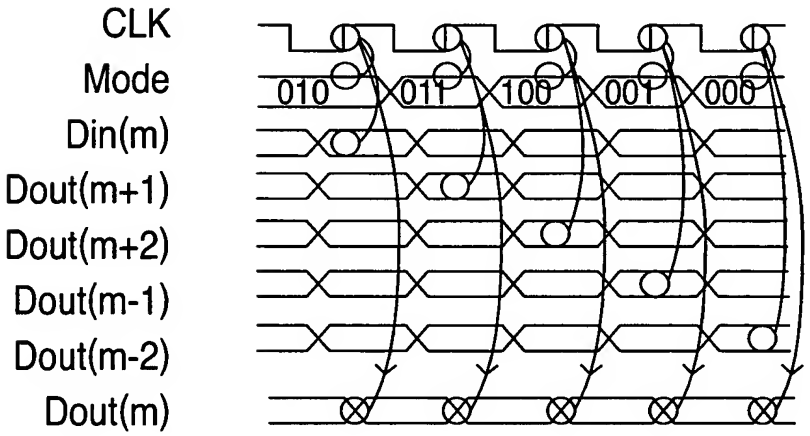
CLK
Mode
Din(m)
Dout(m+1)
Dout(m+2)
Dout(m-1)
Dout(m-2)
Dout(m)
010
011
100
001
000

FIG. 6c

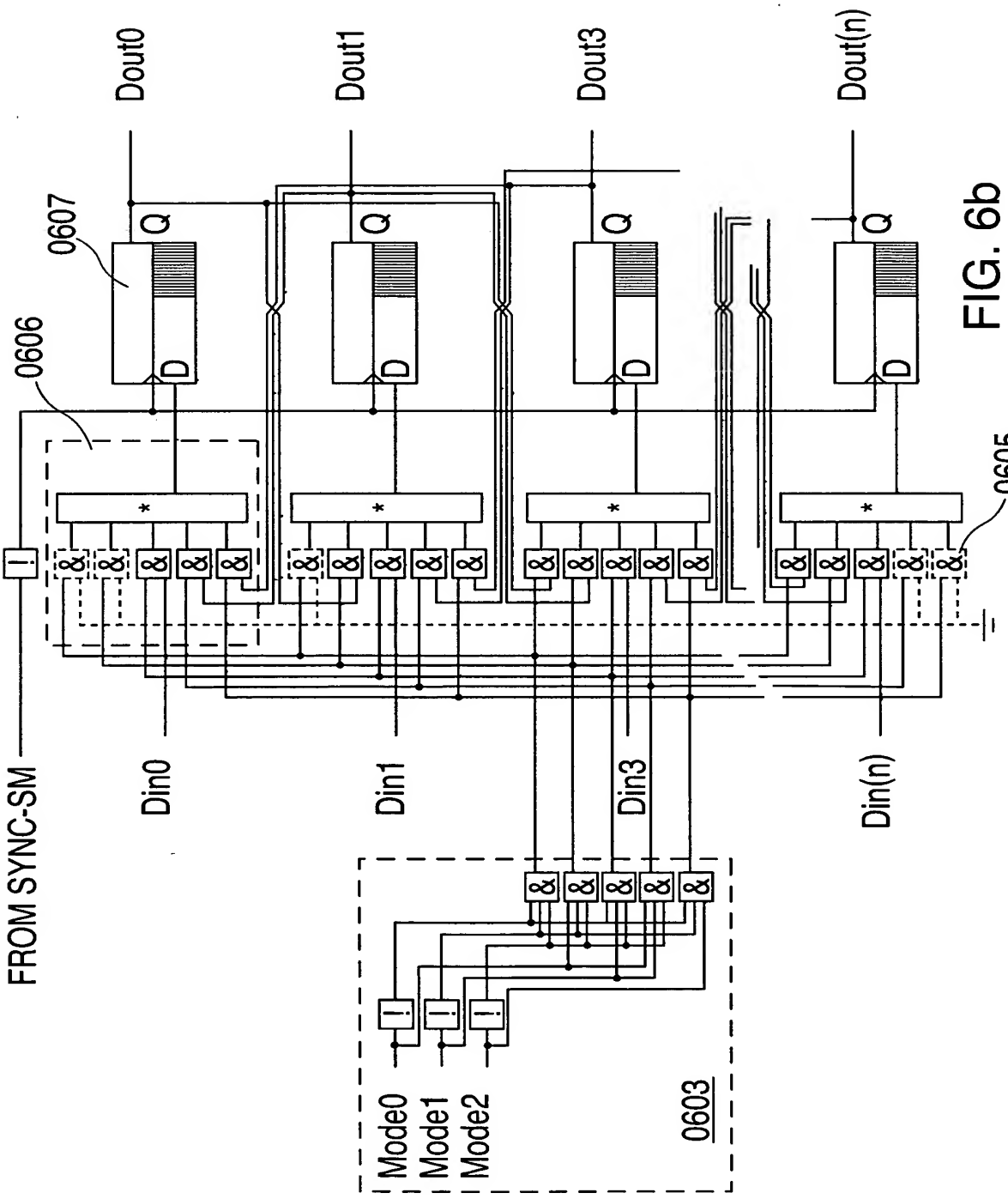
Dout0
Dout1
Dout3
Dout(n)
0607
Q
D
0606
0605
FROM SYNC-SM
Din0
Din1
Din3
Din(n)
Mode0
Mode1
Mode2
0603

FIG. 6b

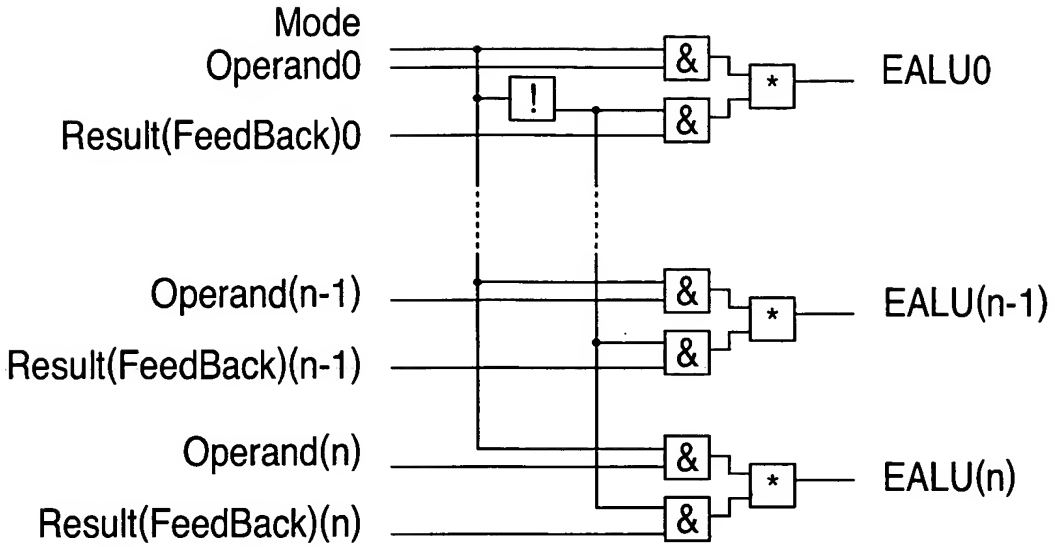
Mode
Operand0
Result(FeedBack)0
Operand(n-1)
Result(FeedBack)(n-1)
Operand(n)
Result(FeedBack)(n)
&
!
*
EALU0
EALU(n-1)
EALU(n)

FIG. 7a

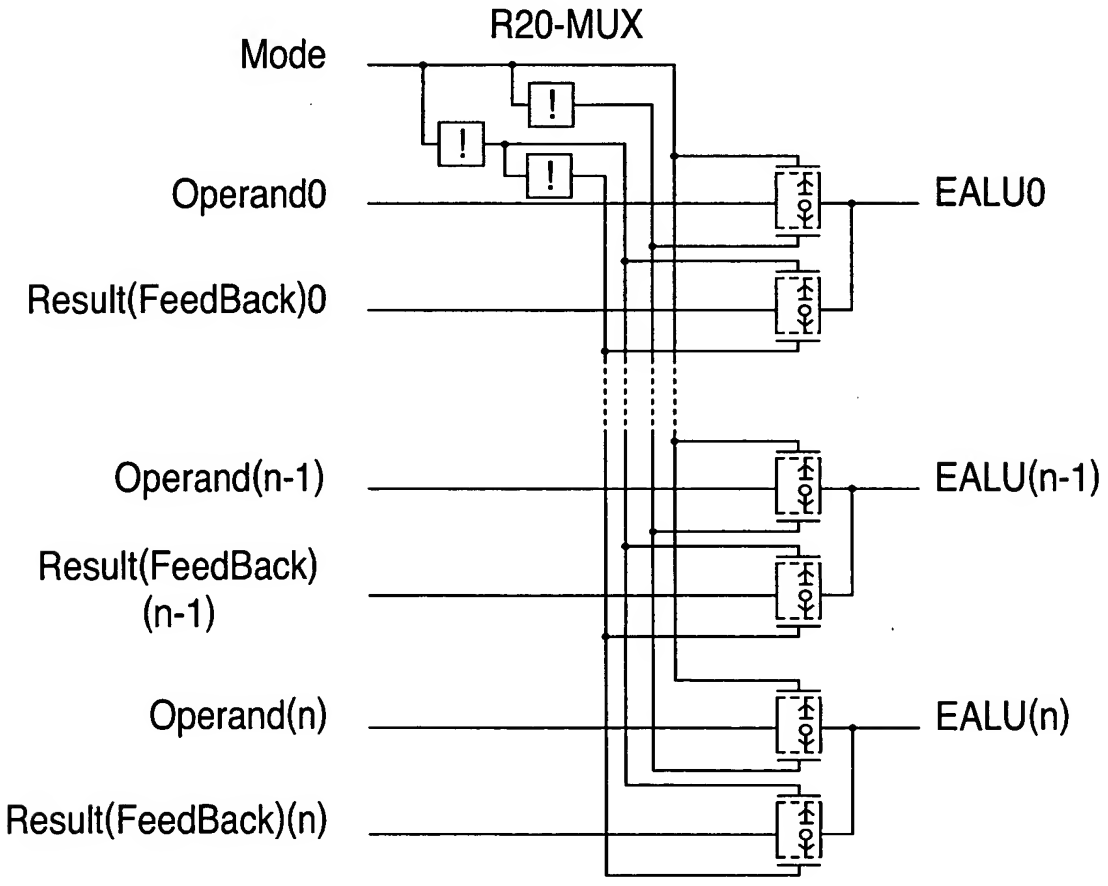
R20-MUX
Mode
Operand0
Result(FeedBack)0
Operand(n-1)
Result(FeedBack)
(n-1)
Operand(n)
Result(FeedBack)(n)
!
EALU0
EALU(n-1)
EALU(n)

FIG. 7b

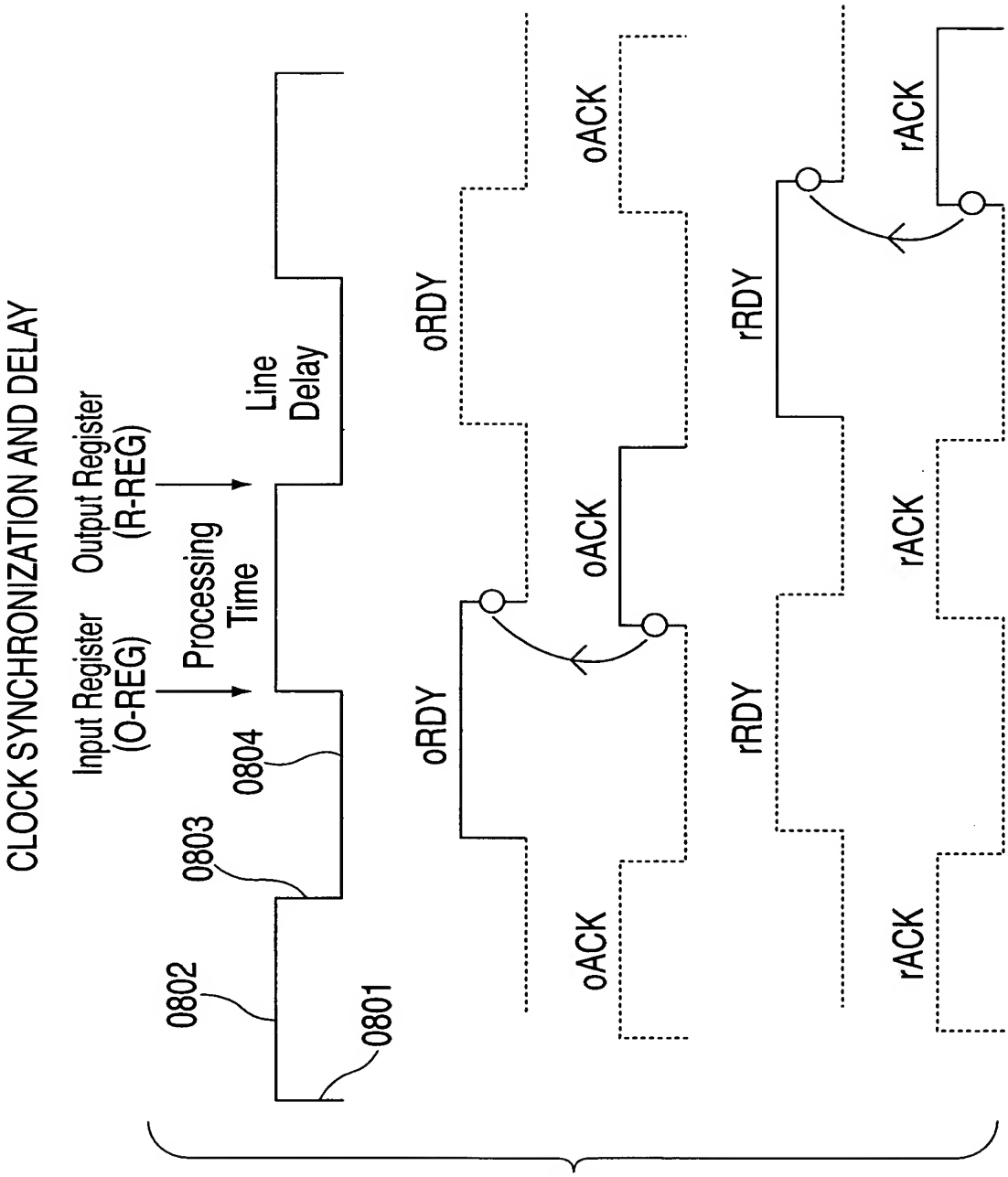
CLOCK SYNCHRONIZATION AND DELAY
Input Register (O-REG)
Processing Time
Output Register (R-REG)
Line Delay
0801
0802
0803
0804
oRDY
oACK
oRDY
oACK
rRDY
rACK
rRDY
rACK

FIG. 8

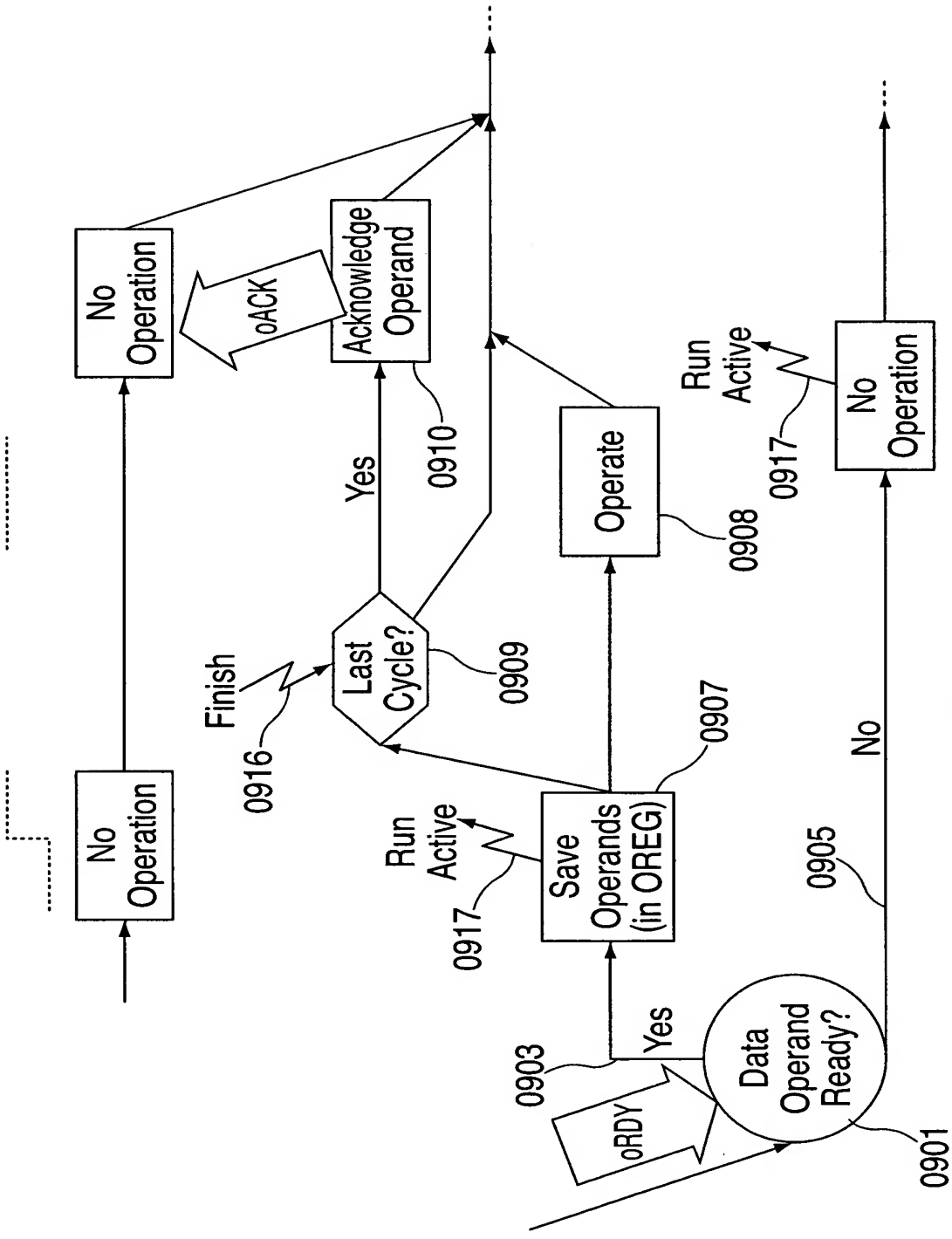
No Operation
No Operation
oACK
Acknowledge Operand
0910
Yes
Finish
0916
Last Cycle?
0909
Operate
0908
Run Active
0917
No Operation
Run Active
0917
Save Operands (in OREG)
0907
No
0905
0903
Yes
oRDY
Data Operand Ready?
0901

FIG. 9/1

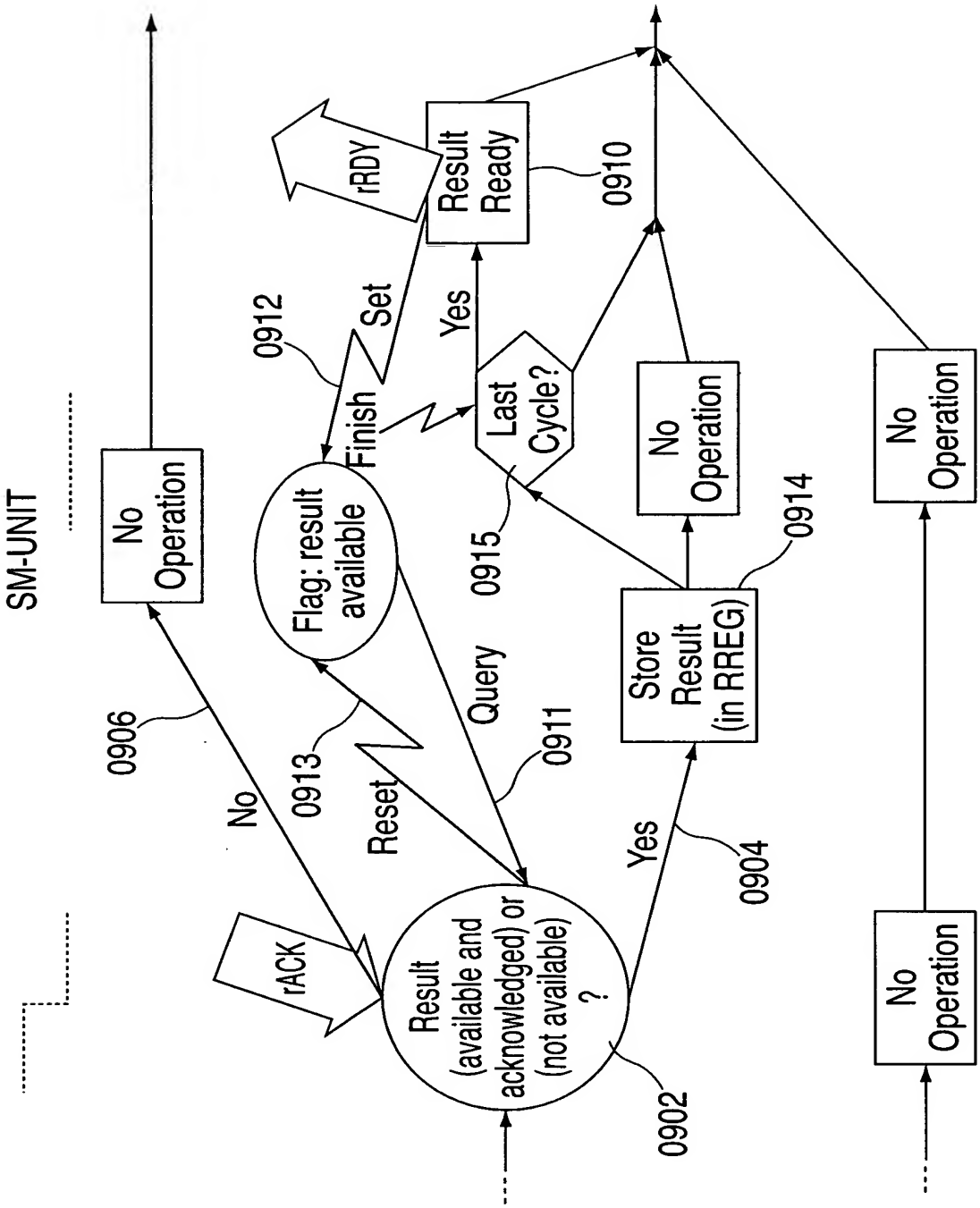
SM-UNIT
No Operation
0906
No
rACK
Result (available and acknowledged) or (not available) ?
0902
Reset
0913
Flag: result available
Query
0911
Finish
Set
0912
rRDY
Result Ready
0910
Yes
Last Cycle?
0915
Yes
0904
Store Result (in RREG)
0914
No Operation
No Operation
No Operation

FIG. 9/2

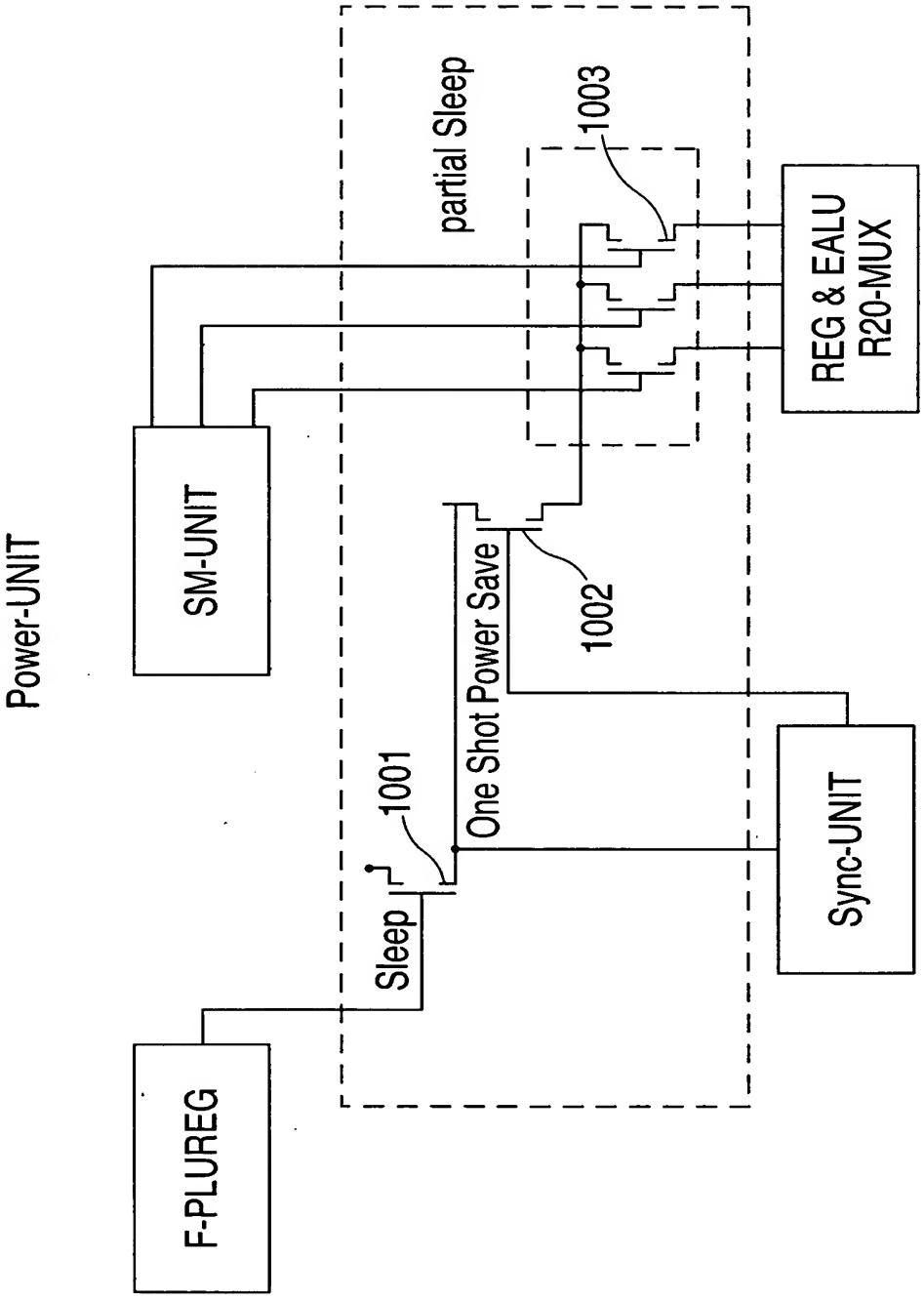
Power-UNIT
F-PLUREG
SM-UNIT
partial Sleep
Sleep
1001
One Shot Power Save
1002
1003
REG & EALU
R20-MUX
Sync-UNIT

FIG. 10

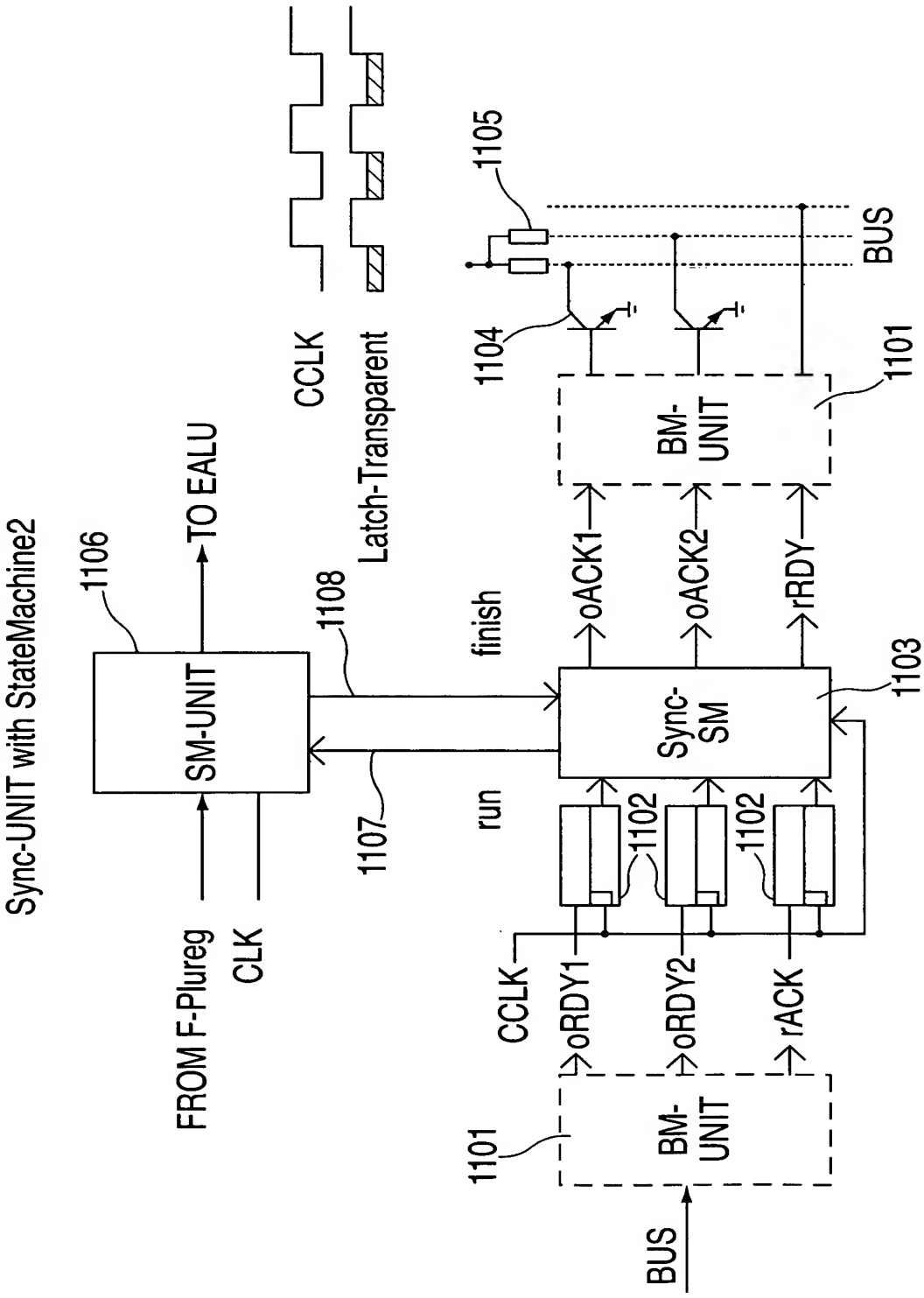
Sync-UNIT with StateMachine2
1106
TO EALU
SM-UNIT
FROM F-Plureg
CLK
1108
1107
Latch-Transparent
CCLK
finish
run
1105
1104
BUS
BM-UNIT
1101
oACK1
oACK2
rRDY
Sync-SM
1103
1102
1102
CCLK
oRDY1
oRDY2
rACK
1101
BM-UNIT
BUS

FIG. 11

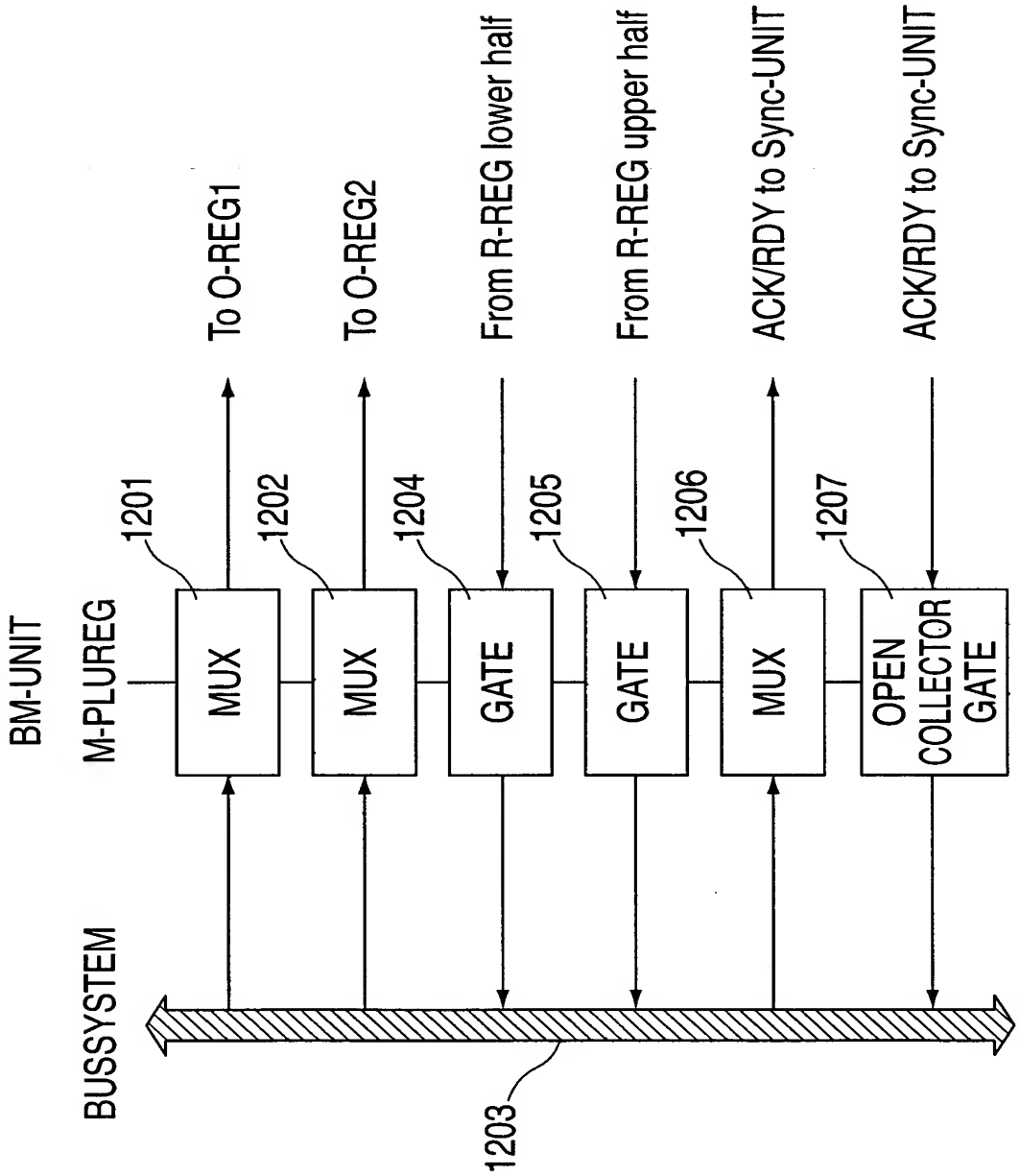
BM-UNIT
M-PLUREG
BUSSYSTEM
MUX
MUX
GATE
GATE
MUX
OPEN COLLECTOR GATE
1201
1202
1204
1205
1206
1207
1203
To O-REG1
To O-REG2
From R-REG lower half
From R-REG upper half
ACK/RDY to Sync-UNIT
ACK/RDY to Sync-UNIT

FIG. 12

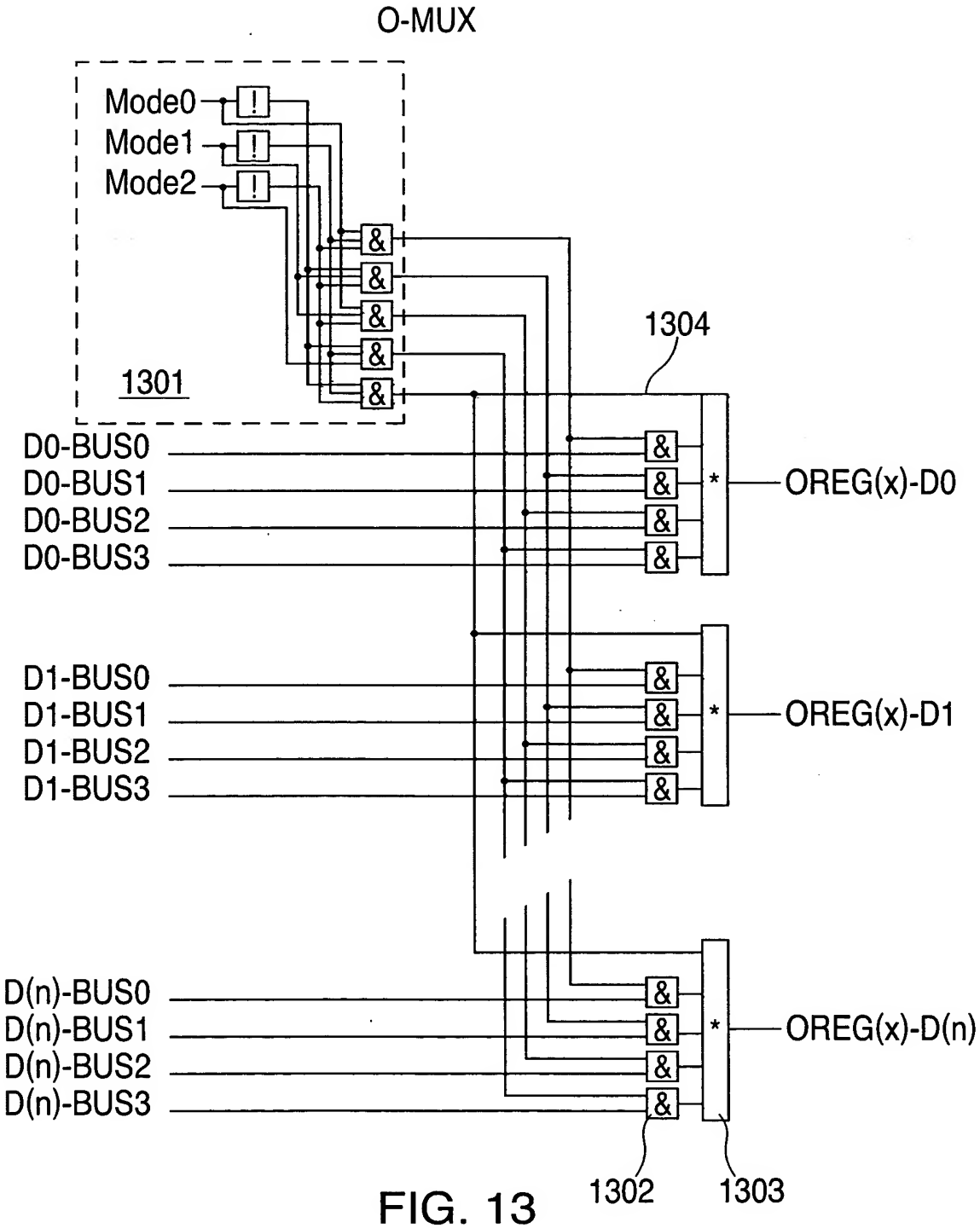
O-MUX
Mode0
Mode1
Mode2
1301
1304
D0-BUS0
D0-BUS1
D0-BUS2
D0-BUS3
OREG(x)-D0
D1-BUS0
D1-BUS1
D1-BUS2
D1-BUS3
OREG(x)-D1
D(n)-BUS0
D(n)-BUS1
D(n)-BUS2
D(n)-BUS3
OREG(x)-D(n)
1302
1303

FIG. 13

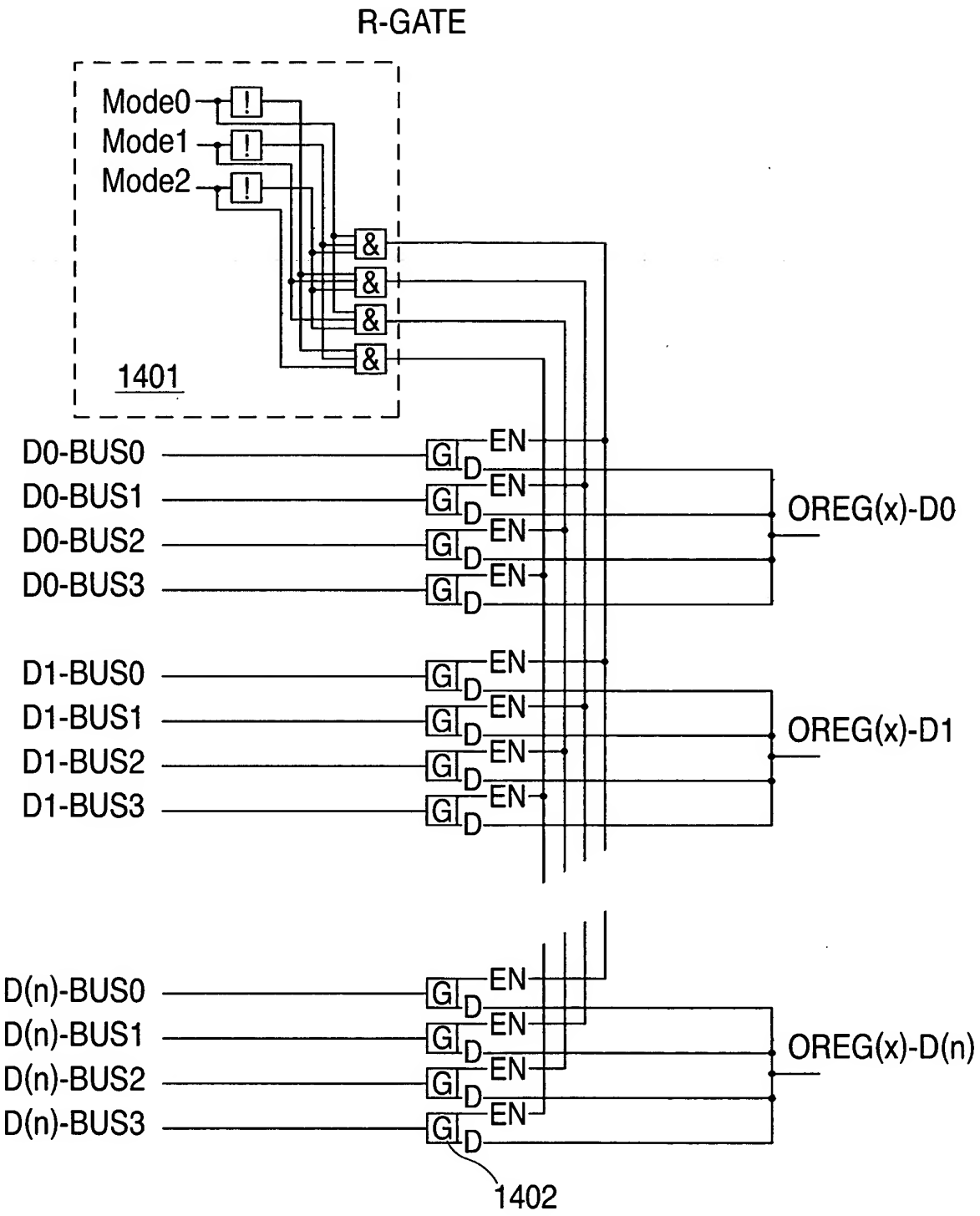
R-GATE
Mode0
Mode1
Mode2
!
!
!
&
&
&
&
1401
D0-BUS0
D0-BUS1
D0-BUS2
D0-BUS3
D1-BUS0
D1-BUS1
D1-BUS2
D1-BUS3
D(n)-BUS0
D(n)-BUS1
D(n)-BUS2
D(n)-BUS3
G
D
EN
OREG(x)-D0
OREG(x)-D1
OREG(x)-D(n)
1402

FIG. 14

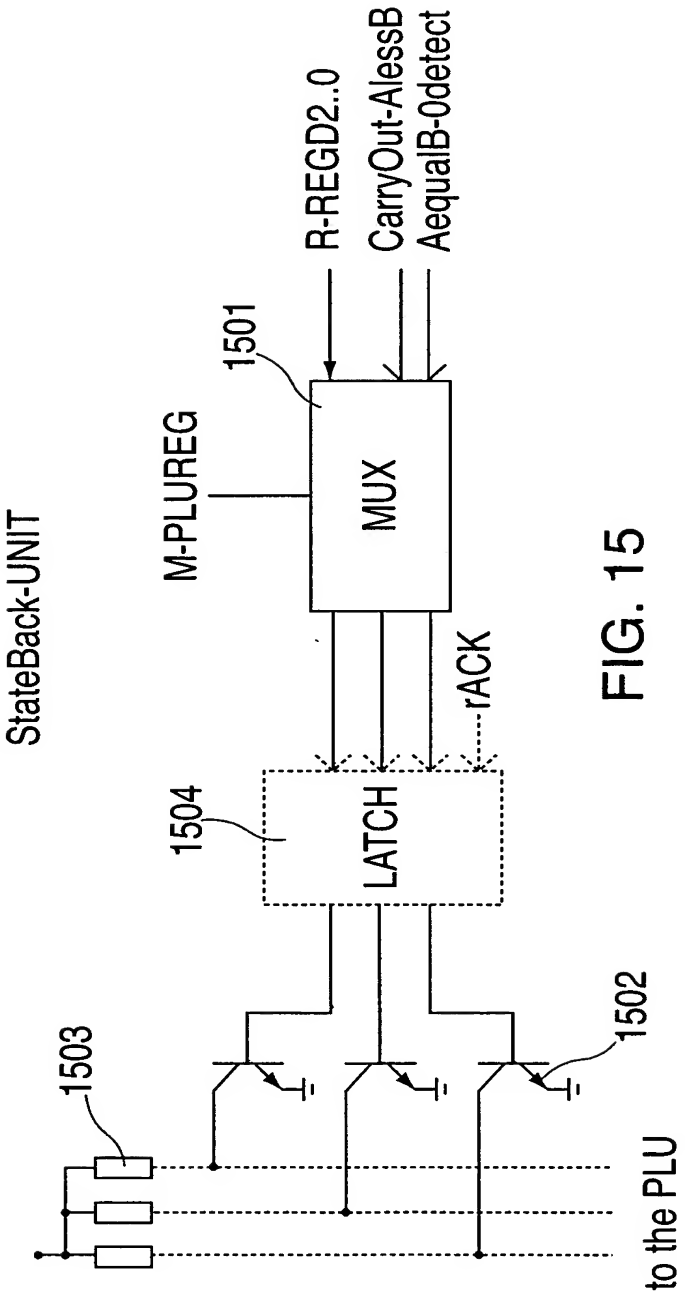
StateBack-UNIT
M-PLUREG
1501
MUX
R-REGD2..0
CarryOut-AlessB
AequalB-0detect
rACK
1504
LATCH
1503
1502
to the PLU

FIG. 15

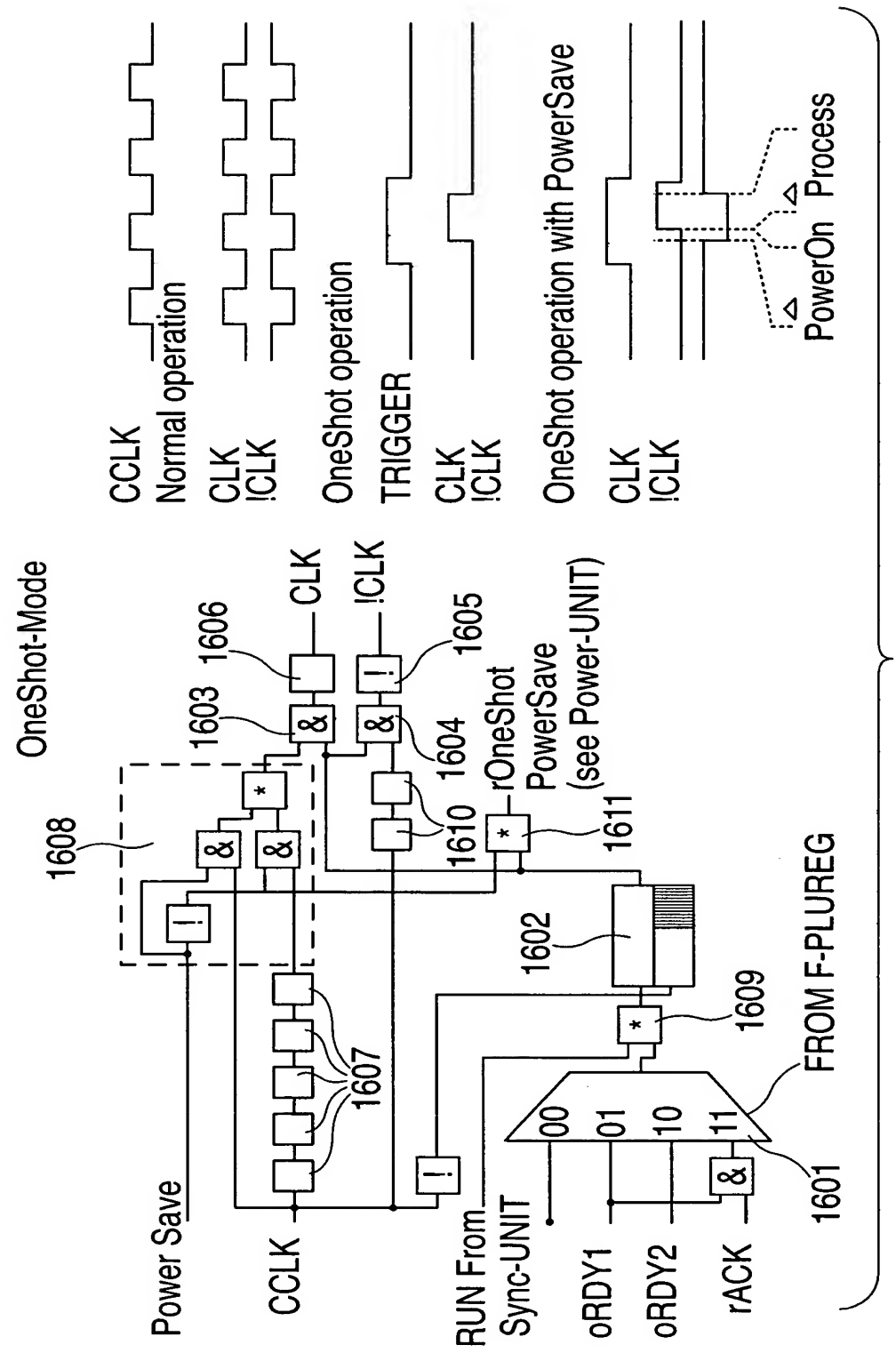
CCLK
Normal operation
CLK
!CLK
OneShot operation
TRIGGER
CLK
!CLK
OneShot operation with PowerSave
CLK
!CLK
PowerOn Process
OneShot-Mode
1608
1603
1606
CLK
!CLK
1605
1604
1610
rOneShot
PowerSave
(see Power-UNIT)
1611
1602
1609
1607
Power Save
CCLK
RUN From
Sync-UNIT
oRDY1
oRDY2
rACK
00
01
10
11
FROM F-PLUREG
1601

FIG. 16

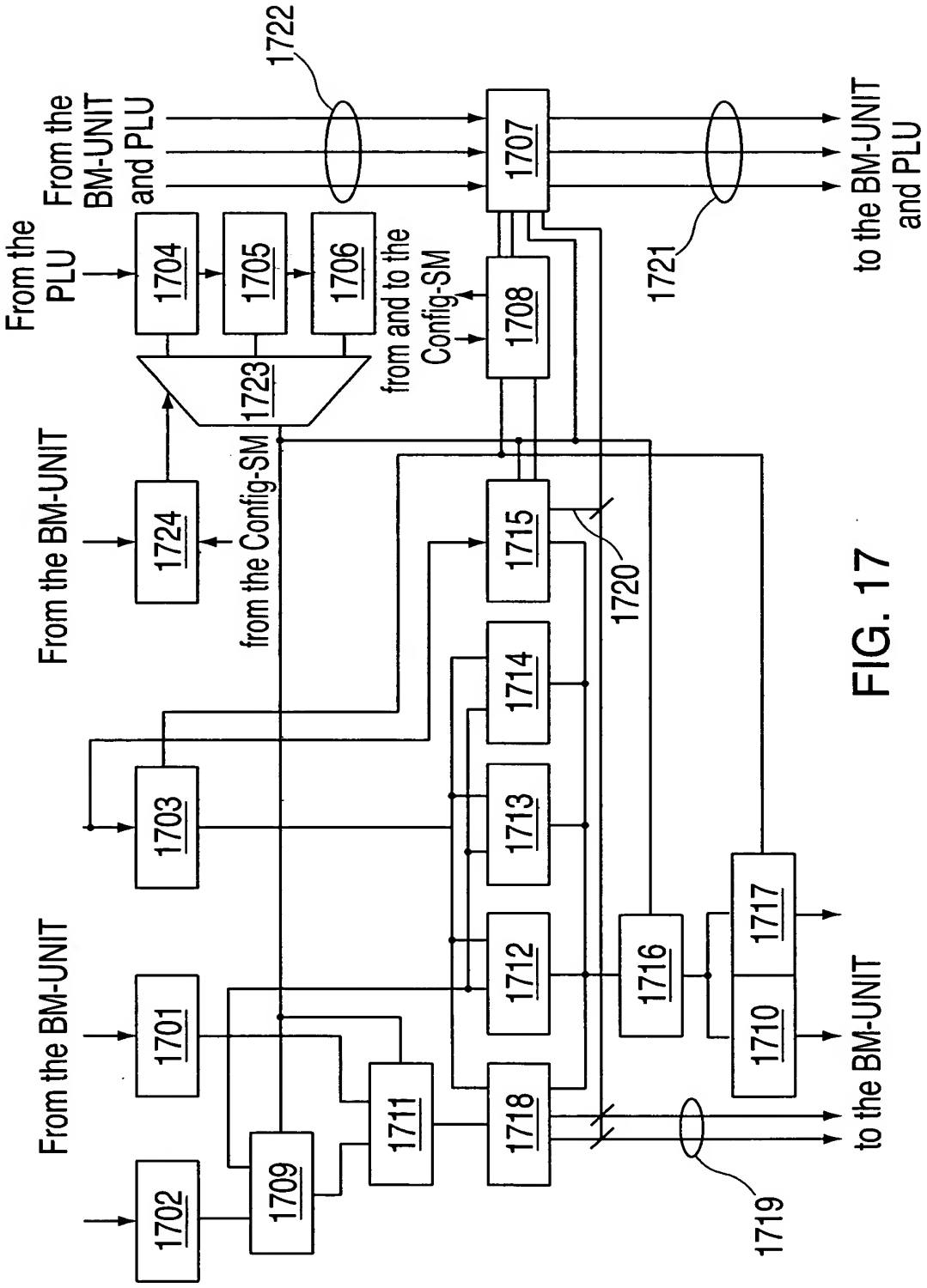
From the BM-UNIT and PLU
1722
1707
From the PLU
1704
1705
1706
1723
from and to the Config-SM
1708
1721
to the BM-UNIT and PLU
From the BM-UNIT
1724
from the Config-SM
1715
1720
1714
1703
1713
From the BM-UNIT
1701
1712
1716
1717
1710
1711
1718
1709
1702
1719
to the BM-UNIT

FIG. 17

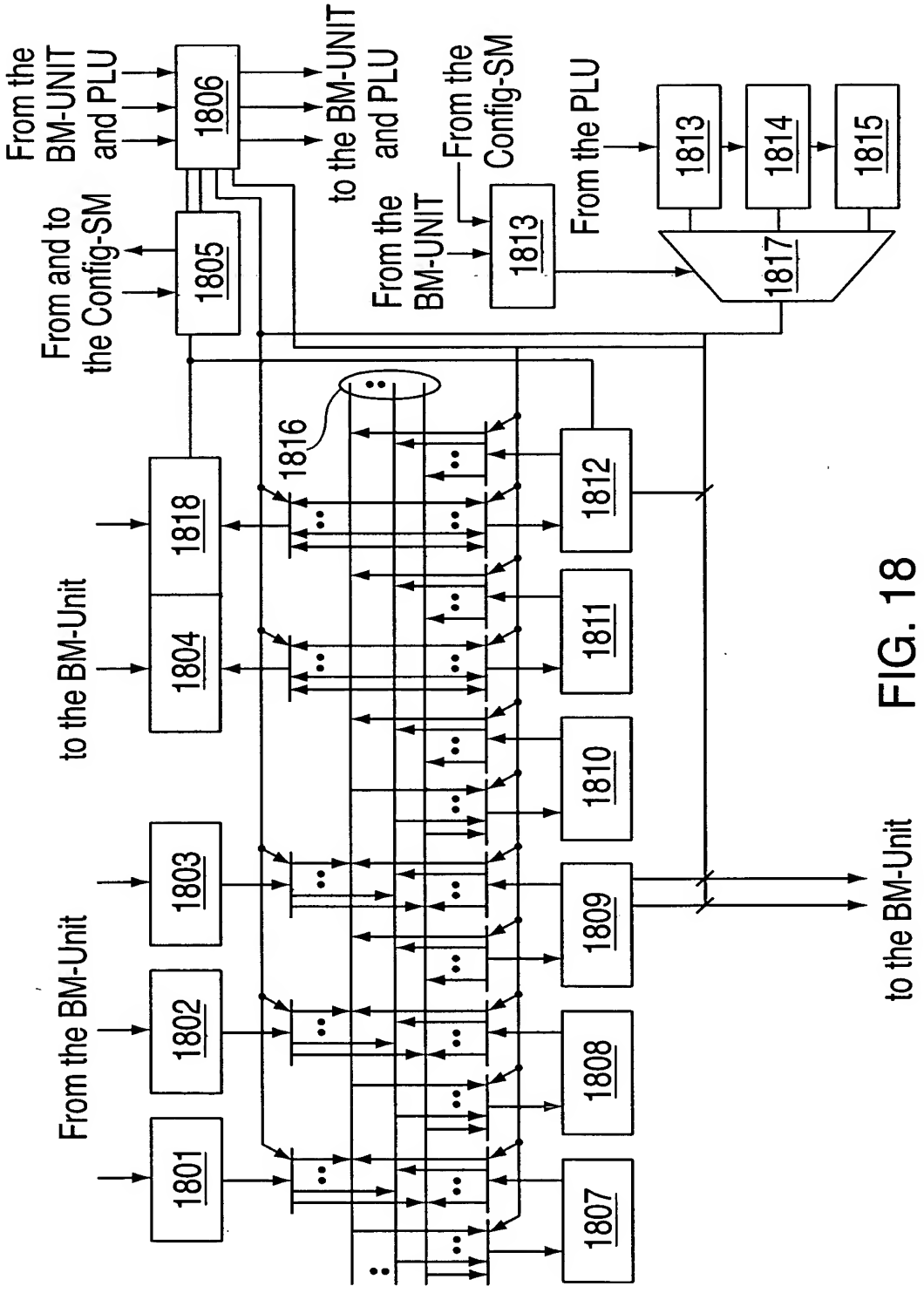
From the BM-UNIT and PLU
1806
to the BM-UNIT and PLU
From and to the Config-SM
1805
From the BM-UNIT
From the Config-SM
1813
From the PLU
1813
1814
1815
1817
1816
1818
1804
1812
1811
1810
1809
1808
1807
1803
1802
1801
to the BM-Unit
From the BM-Unit
to the BM-Unit

FIG. 18

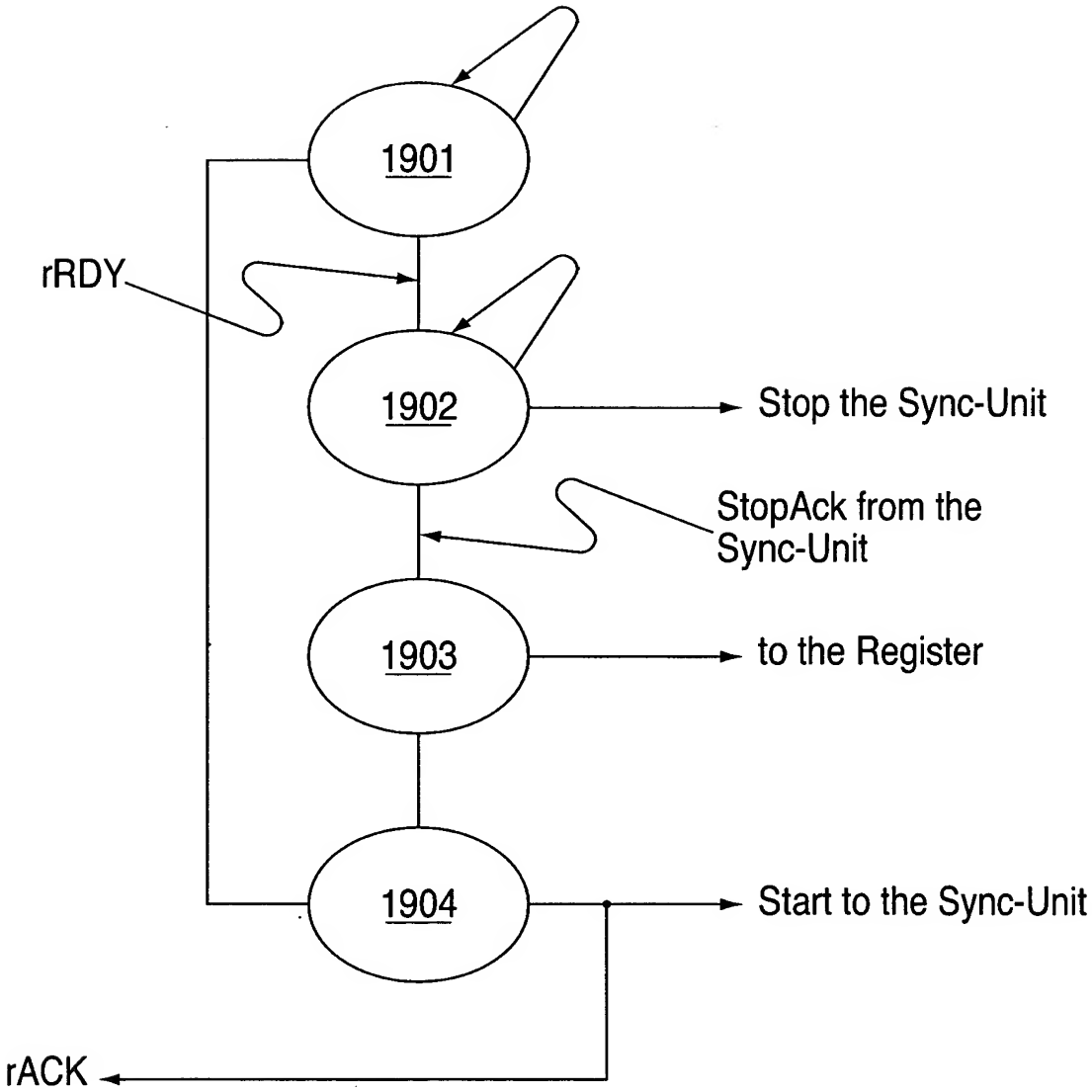
1901
rRDY
1902
Stop the Sync-Unit
StopAck from the
Sync-Unit
1903
to the Register
1904
Start to the Sync-Unit
rACK

FIG. 19

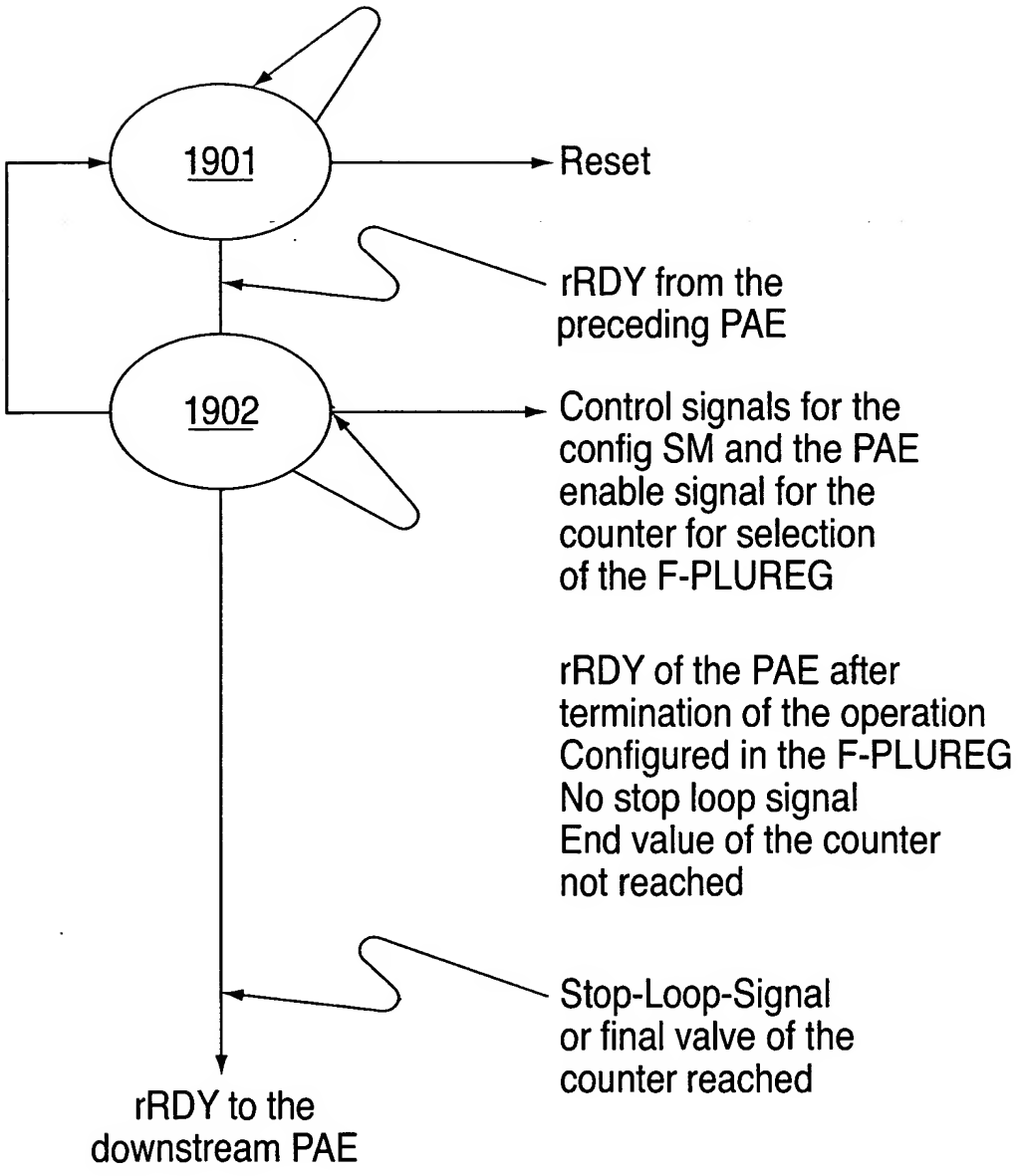
1901
Reset
rRDY from the
preceding PAE
1902
Control signals for the
config SM and the PAE
enable signal for the
counter for selection
of the F-PLUREG
rRDY of the PAE after
termination of the operation
Configured in the F-PLUREG
No stop loop signal
End value of the counter
not reached
Stop-Loop-Signal
or final valve of the
counter reached
rRDY to the
downstream PAE

FIG. 20

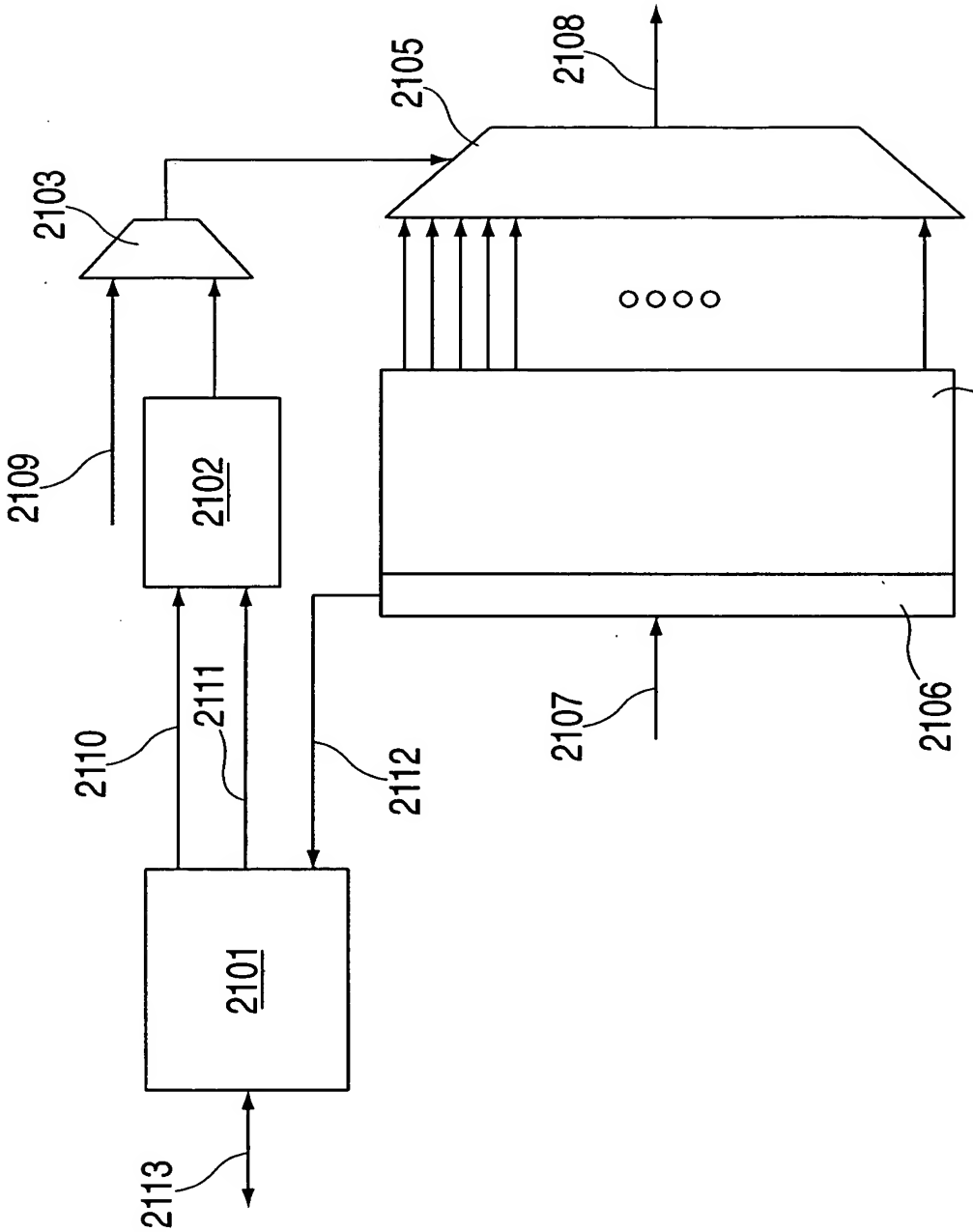
2101
2102
2103
2104
2105
2106
2107
2108
2109
2110
2111
2112
2113

FIG. 21